AMENDMENTS TO THE CLAIMS

1. (previously presented) A driver circuit for controlling upper and lower switching means for converting a direct voltage into a clocked output voltage for a resonant converter with a high-voltage section for controlling the upper switching means and a low-voltage section for controlling the lower switching means which switch the switching means on alternately, the switch-on phases of the switching means being separated from one another by dead-time phases, characterized in that there is provided a first circuit section which controls the duty cycle of the upper switching means as a function of the duty cycle of the lower switching means and receives control signals from the low-voltage section exclusively during the duty cycle of the lower switching means.

2. (previously presented) A driver circuit as claimed in claim 1, characterized in that the first circuit section is equipped with at least one first integrating circuit configuration which is charged during the duty cycle of the lower switching means and discharged during the duty cycle of the upper switching means.

3. (previously presented) A driver circuit as claimed in claim 2, characterized in that the first integrating circuit configuration is equipped with at least one integration capacitor and a charging circuit and a discharging circuit.

4. (previously presented) A driver circuit as claimed in claim 3, characterized in that the charging circuit and the discharging circuit are both equipped with a respective constant-current source.

5. (previously presented) A driver circuit as claimed in claim 2, characterized by a transistor provided in the low-voltage section which transmits a signal to the high-voltage section for the duration of the switch-on of the lower switching means.

6. (previously presented) A driver circuit as claimed in claim 1, characterized by a second circuit section which determines the switch-on instant of the upper switching means as a function of the voltage characteristic of the output voltage.

7. (previously presented) A driver circuit as claimed in claim 6, characterized in that the second circuit section is equipped with a voltage-increase recognition circuit with at least one capacitor, one resistor and one comparator in particular a Schmitt trigger.

8. (previously presented) A driver circuit as claimed in claim 1, characterized by a second circuit section with means which control the duration of the first dead-time phase before the switch-on of the upper switching means as a function of the duration of the second dead-time phase before the switch-on of the lower switching means or by a timer connected to the low-voltage section.

9. (previously presented) A driver circuit as claimed in claim 8, characterized in that the second circuit section is equipped with at least one second integrating circuit configuration which is charged for the duration ΔT_{tot2} of the second dead-time phase, or for the duration of a signal form the external timer, and discharged for the duration of the first dead-time phase.

10. (original) A driver circuit as claimed in claim 9, characterized in that the structure of the second integrating circuit configuration corresponds to the structure of the first integrating circuit configuration.

11. (previously presented) A driver circuit as claimed in claim 1, characterized by a voltage-decrease recognition circuit with at least one capacitor, one resistor and one comparator especially a Schmitt trigger, for determining the switch-on instant t_{ein4} for the lower switching means.

12. (previously presented) A resonant converter with a driver circuit for controlling upper and lower switching means for converting a direct voltage into a clocked output voltage for the resonant converter with a high-voltage section for controlling the upper switching means and a

low-voltage section for controlling the lower switching means which switch the switching means on alternately, the switch-on phases of the switching means being separated from one another by dead-time phases, characterized by a first circuit section, which controls the duty cycle of the upper switching means as a function of the duty cycle of the lower switching means and receives control signals from the low-voltage section exclusively during the duty cycle of the lower switching means.